WHAT IS CLAIMED IS:

1. A method of operating a parallel computer system having at least two processor elements and having a distributed memory, each processor element comprising a local program memory, data memory, communications memory and an operating system, the method comprising the steps of

(a) in each processor element, globally writing global data and locally reading global data,

(b) adjoining a global address and/or a number to data written globally,

(c) for each processor element, determining with an address and/or a number comparator in each processor element on the basis of the address whether the particular processor element is interested in data written globally,

(d) determining with a local address computation unit a physical address in processor memory when the processor element is interested in the data, and

(e) establishing parameters of the address and/or number comparator and of the address computation unit in each processor element before or during processing with the operating system.

2. A method according to claim 1 including controlling the exchange of messages with a communications manager unit to make possible "zero copying".

3. A method according to claim 1 wherein the address comparator comprises one or more address windows, each window

comprising an initial address (base) and an end address (top) and that all data within one of these windows are processed further locally.

4. A method according to claim 1 including dividing global address space into pages and defining with a table in the address comparator which data are to be processed further locally.

5. A method according to claim 4 including adding an offset of one or more bits to a global address to determine a local address.

6. A method according to claim 4 including replacing one or more bits of the global address by a base value to determine a local address.

7. A method according to claim 4 including forming the table from one or more bits of the global address and/or number and entering a local address value co-determining the address for each table entry.

8. A method according to claim 1 including selectively transmitting global writing to selected groups of less than all processors in the system, thereby substantially reducing load on the network.

9. A method according to claim 1 wherein barrier synchronization, wherein all processor elements have reached a hit point, is supported by a communications manager unit.

10. A method according to claim 1 including transferring event recognition by a single processor through a communications manager unit to the entire system.

11. A method according to claim 1 including supporting one or more exclusive keys with a communications manager unit.

12. A method according to claim 1 wherein one or more processor elements act directly as input and/or output elements.

13. A parallel computer system comprising

at least two processor elements with distributed memory, each processor element comprising a local program memory, a data memory, a communications unit for writing data globally and reading data locally, a communications memory and an operating system, each processor element including a communications manager unit to control the communications unit.

14. A parallel computer system according to claim 13 wherein each communications manager unit is inserted between each communications unit and a local data transport system of each processor element.

15. A parallel computer system according to claim 13 wherein each communications manager unit comprises an address comparator and an address computation unit.